C1 cont

7. (Amended) A semiconductor device according to claim 11 wherein said diffusion layer of the first conductivity type is a channel stopper region.

8. (Amended) A semiconductor device according to claim 12 wherein said diffusion layer of the first conductivity type is a channel stopper region.

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11. (Amended) A semiconductor device according to claim 13, wherein said transistor is a high voltage transistor, said source diffusion layer and said drain diffusion layer are high impurity concentration, and said source side offset diffusion layer and said drain side offset diffusion layer are lower in impurity concentration than said source diffusion layer and said drain diffusion layer.

12. (Amended) A semiconductor device according to claim 14, wherein said transistor is a high voltage transistor, said source diffusion layer and said drain diffusion layer are high impurity concentration, and said source side offset diffusion layer and said drain side offset diffusion layer are lower in impurity concentration than said source diffusion layer and said drain diffusion layer.

Please add new claims 13 and 14 as follows:

--13. A semiconductor device comprising:

a source side offset diffusion layer region and a drain side offset diffusion layer region of a second conductivity type in a transistor formed, so as to be separated from each other, in a predetermined in a region of a first conductivity type in a semiconductor substrate;

a gate insulator film region formed between said source side offset diffusion layer region and said drain side offset diffusion layer region; a gate electrode formed on said gate insulator film region; and

a diffusion layer of the first conductivity type of which the impurity concentration is higher than that of said region of the first conductivity type and which is formed so as to surround said source side offset diffusion layer region, said drain side offset diffusion layer region and said gate insulator film region, wherein both ends of said gate insulator film region, in the channel width direction in the plan view, form protruding portions that protrude at the borders of said source side offset diffusion layer region and of said drain side offset diffusion layer region in the direction toward said diffusion layer of the first conductivity type, and wherein said diffusion layer of the first conductivity type is formed so as not to be substantially

"in the plan view"
"in a plan view"

present below said gate insulator film region and formed so as to be in contact with said protruding portions.

14. A semiconductor device comprising:

a source side offset diffusion layer region and a drain side offset diffusion layer region of a second conductivity type in a transistor formed, so as to be separated from each other, in a predetermined region in a region of a first conductivity type in a semiconductor substrate;

a gate insulator film region formed between said source side offset diffusion layer region and said drain side offset diffusion layer region; a gate electrode formed on said gate insulator film region; and

a diffusion layer of the first conductivity type of which the impurity concentration is higher than that of said region of the first conductivity type and which is formed so as to surround said source side offset diffusion layer region, said drain side offset diffusion layer region and said gate insulator film region, wherein both ends of said gate insulator film region, in the channel width direction in the plan view, form protruding portions that, protrude at the borders of said source side offset diffusion layer region and of said drain side offset diffusion layer region in the direction toward said diffusion layer of the

first conductivity type, and wherein said diffusion layer of the first conductivity type is formed so as to surround said protruding portions and so as to be separated from the protruding portions by a predetermined distance.--

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395-400
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333 ?
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